



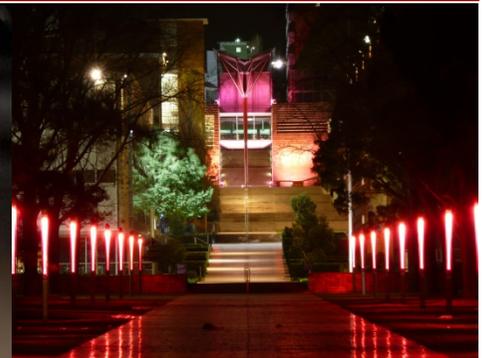
# Patterning for Plated Heterojunction Cells

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Never Stand Still

Faculty of Engineering

Photovoltaic and Renewable Energy Engineering

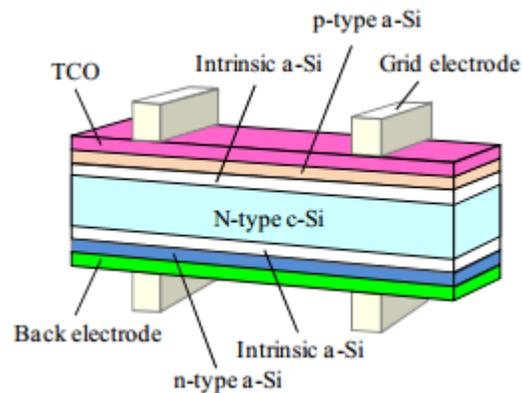


# Content

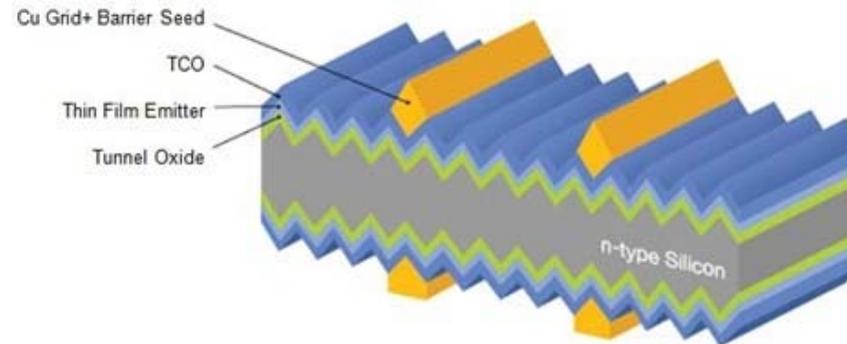
- **Motivation**
- **Patterning Process**
- **Results for Patterning and Plating**
- **Direct Cu Plated Bifacial Si-HJT Cells**
- **Conclusions**

# Motivation

- Carrier selective contacts silicon cells (e.g., heterojunction and passivated contact cells) are attracting much interest.
- However they typically require low temperature metallisation.
- Furthermore the cell structure is amenable to bifaciality.
- So need low-cost technology for patterning (masking) and bifacial cell plating. **Low-cost masking is challenging to achieve.**

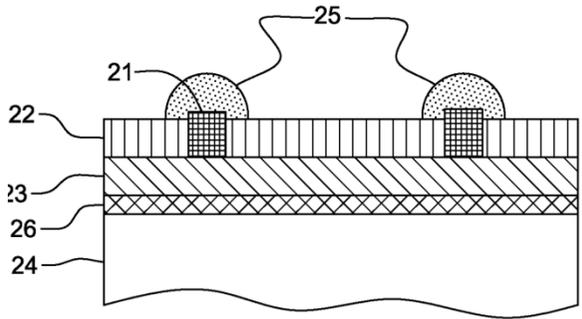


Schematic view of a Heterojunction with Intrinsic Thin-layer (HIT) solar cell<sup>1</sup>

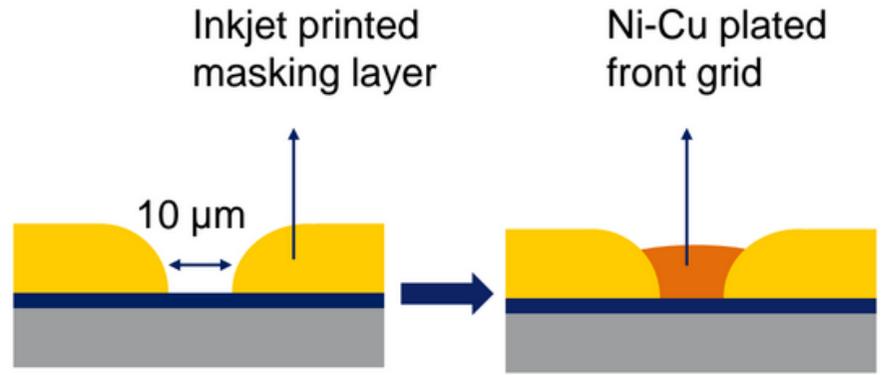


Tunnel Oxide Junction Bifacial Solar Cell with Electroplated Cu Gridlines<sup>2</sup>

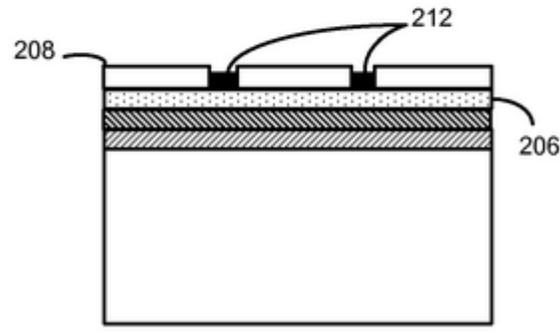
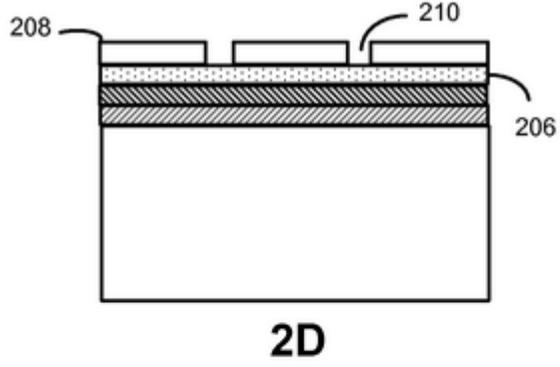
# Existing Approaches for Masking



Use a laser to convert a functional layer to be metallic<sup>1</sup>



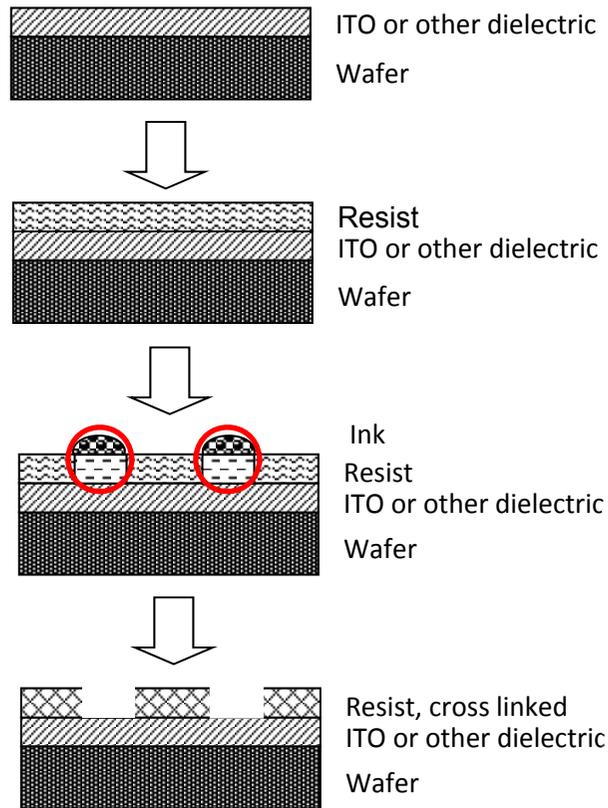
Printing hot melt ink as a mask<sup>3</sup>



Screen printing a mask leaving openings in the mask for metal contacts<sup>2</sup>

1 US Patent, US20120060908  
 2 US Patent, US20130125974  
 3 J.P. Hermans et al., *Proceedings of 29<sup>th</sup> EUPVSEC*, Amsterdam, 2014

# Patterning Process Used for This Work



1. Apply resist

2. Print ink

3. Bake

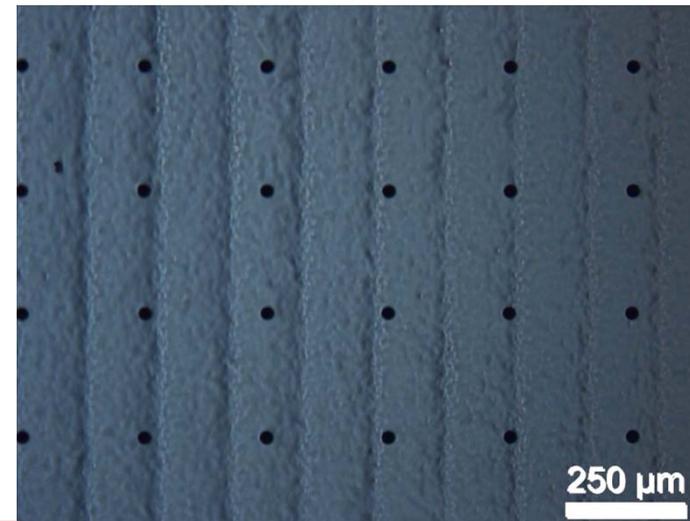
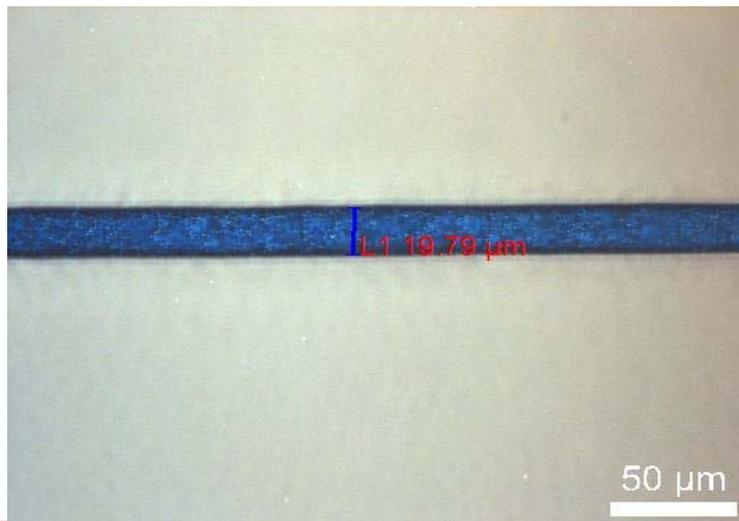
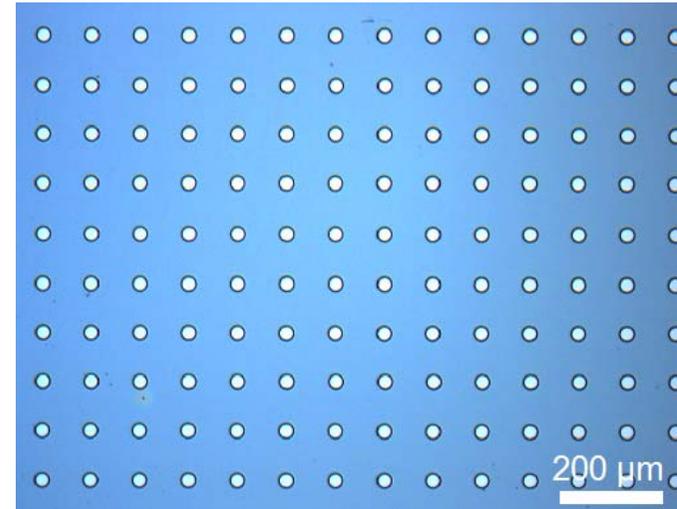
4. Develop



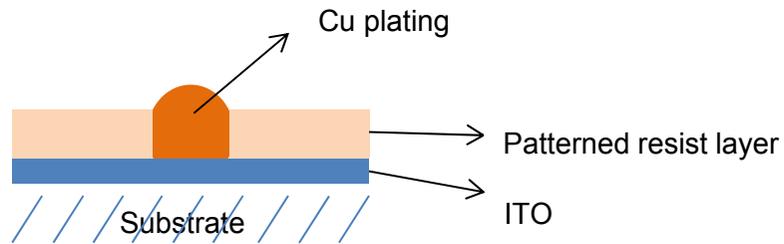
Demonstrated for  
156 mm wafers

# Patterning Results

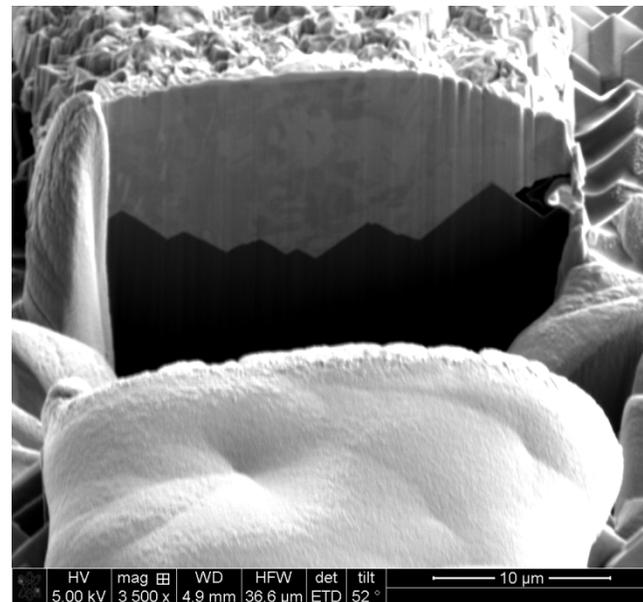
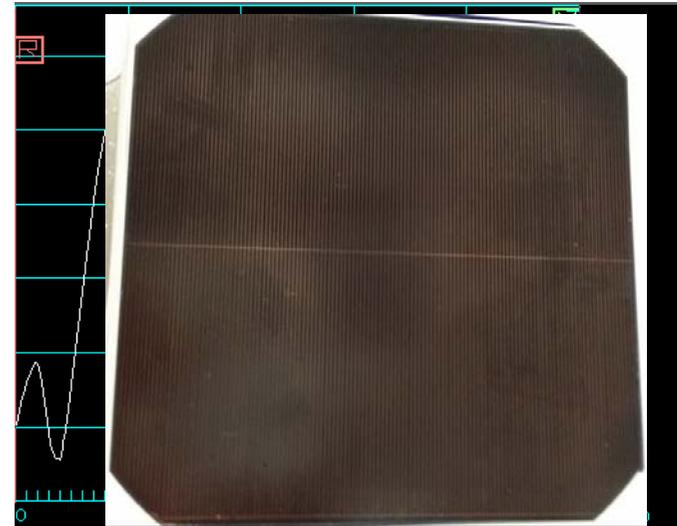
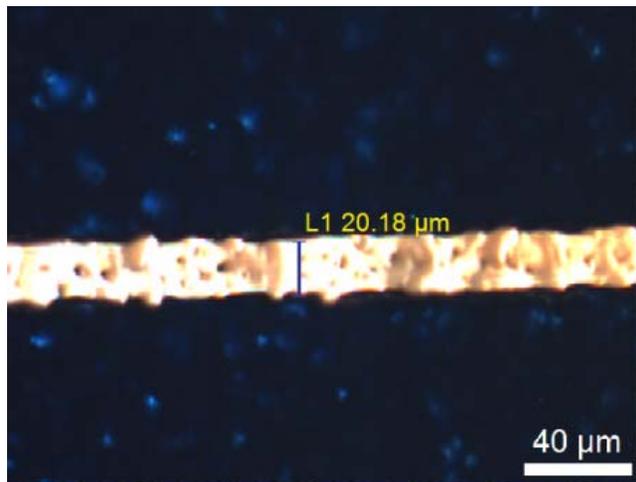
- Fine structures can be formed by this technique.
- On textured wafer surfaces, line openings with a width of  $< 20 \mu\text{m}$  and point openings with a diameter of  $\sim 20 \mu\text{m}$  can be formed.



# Plating Results



Plated fingers after Sn capping with 26  $\mu\text{m}$  width and 10  $\mu\text{m}$  height can be formed.

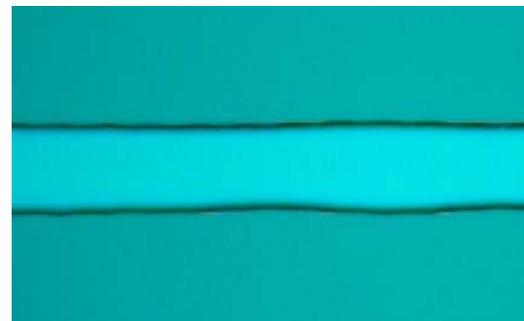
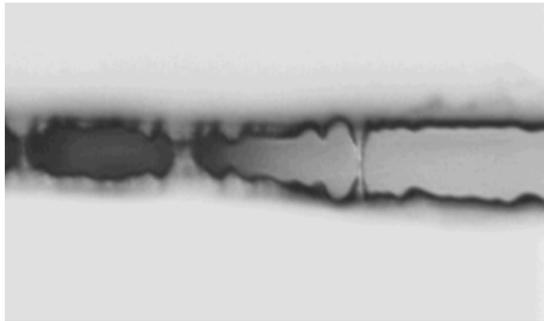


# Comparison with Photolithography

|              | Photolithography   | This Method   |
|--------------|--|---|
| Steps        | Several steps  | No UV exposure, no soft baking required   |
| Equipment    | Mask aligner, mask, UV light,  | Inkjet printer  |
| Materials    | Resist (resin) with photo-active component   | Resin without photosensitive component, ink with a complexity equivalent to graphic art ink                                       |
| Environment  | Need clean room (large particles in the air can block the light and affect patterning) | No clean room environment necessary   |
| Feature size | Several $\mu\text{m}$ if an expensive optical lens is not used                         | $\sim 20 \mu\text{m}$ (resolution limited by the printer). Point openings as small as $5 \mu\text{m}$ in diameter can be achieved |

# Other Features

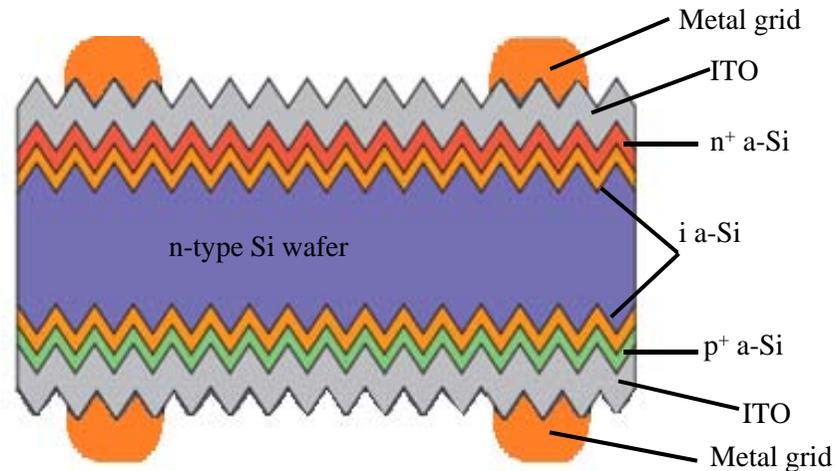
- **Fast** Only one layer of ink (1 pL droplets) is required to be printed. Throughput of 2400 wafers/hr quoted for PiXDRO JETx platform.
- Clear sharp edges after developing the resist.



“Mouse bites” edge (can occur with photolithography)    Clear patterned edge

- Low temperature process. The baking temperature is  $< 140^\circ \text{C}$ .
- Large process window. Robust to variations in resist thickness. Resist as thick as  $10 \mu\text{m}$  can be patterned using 1 layer of ink.

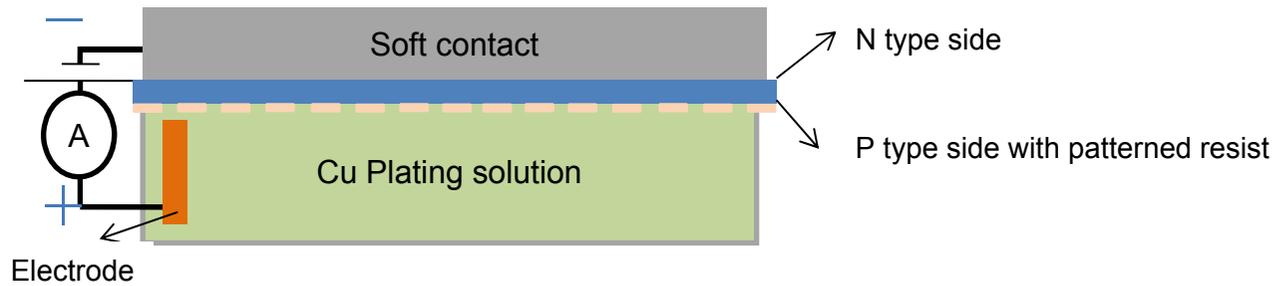
# Application to Bifacial HJT Cells



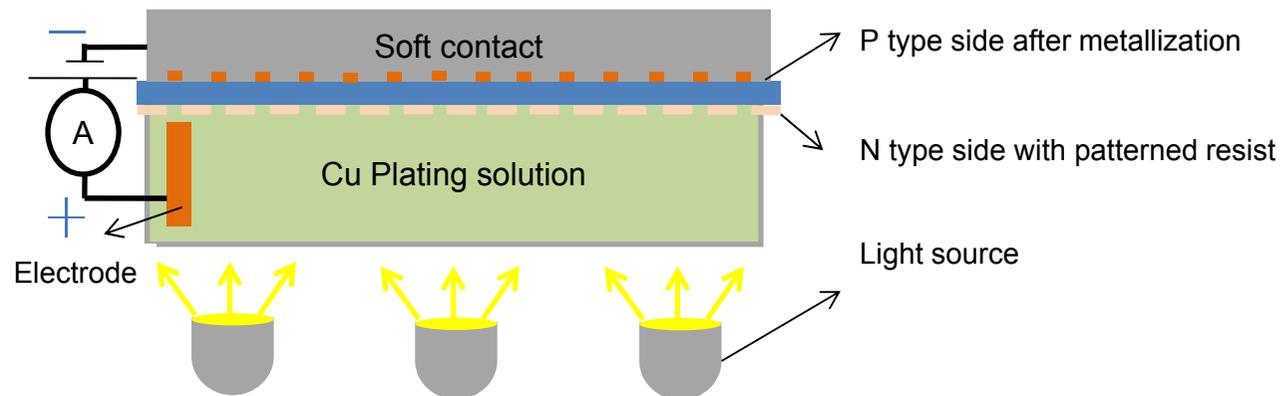
- Low temperature metallisation is desirable for HJT cells,
- Bifacial cells require that the masking and plating process can be applied to both p-type and n-type surfaces.
- Can mask and plate:
  1. Busbar/finger patterns (with traditional interconnection); or
  2. Fingers and interconnect with SmartWire or MultiBB

# Bifacial Cell Plating

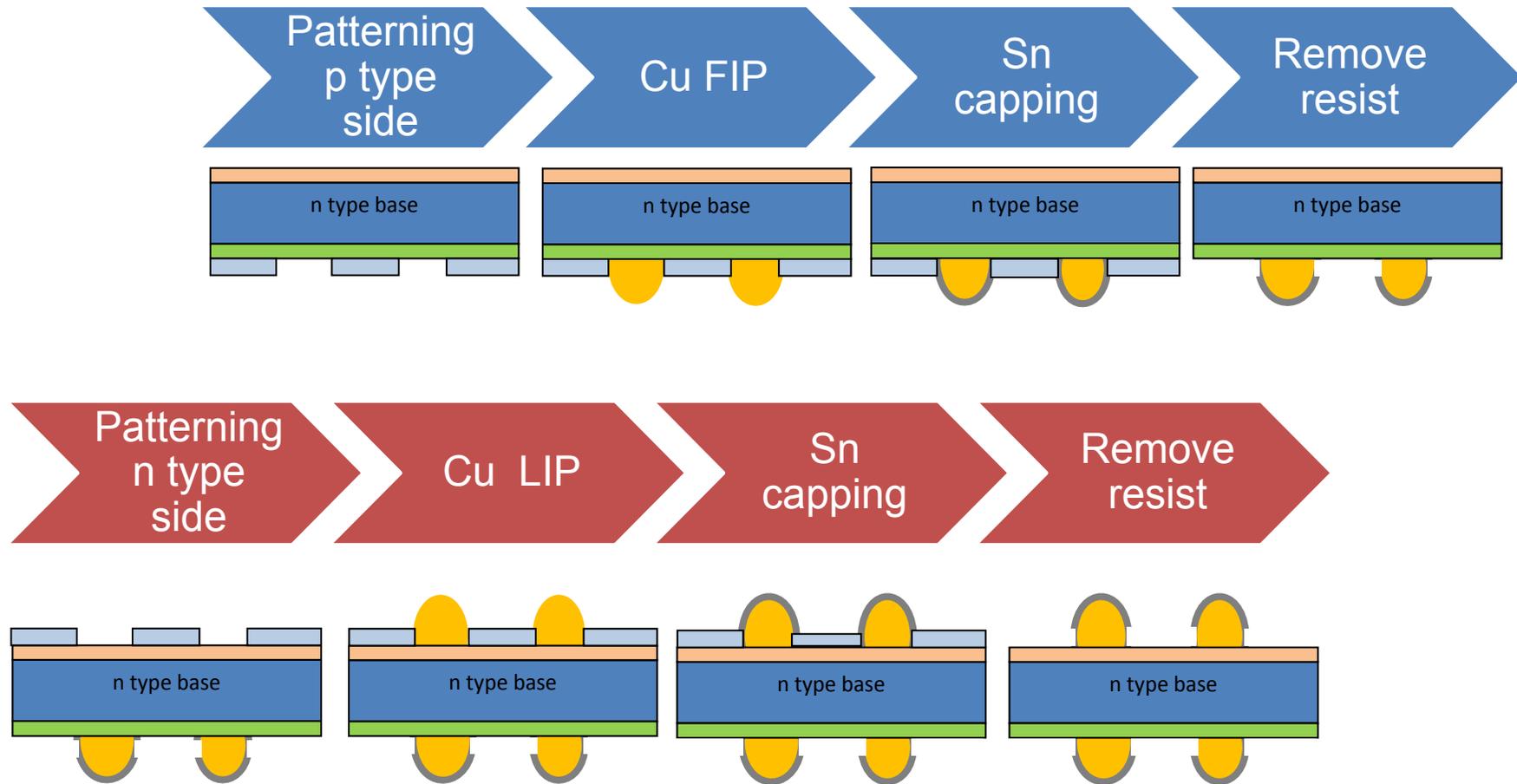
- Field-induced plating (FIP; also called forward bias plating) to plate to p-type surface



- Bias-assisted light induced plating (LIP) to plate to n-type surface

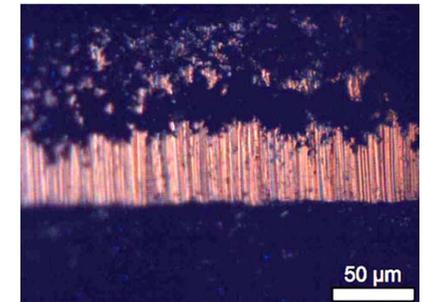
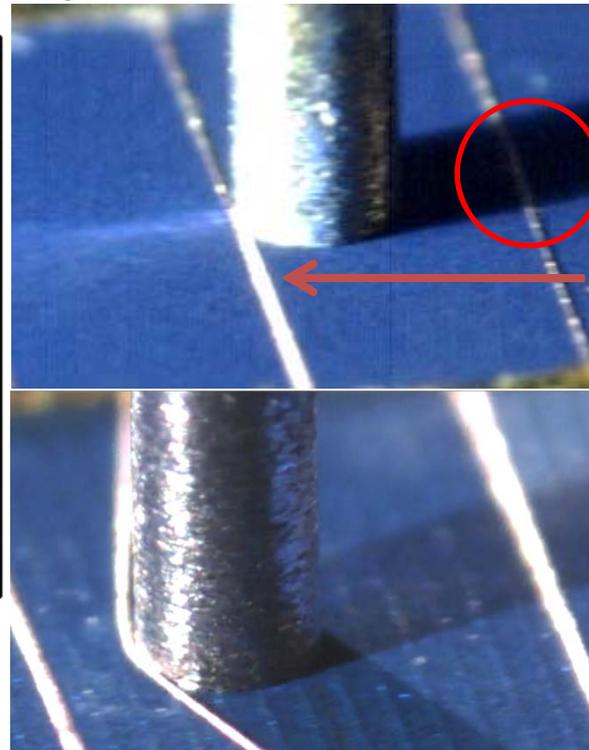
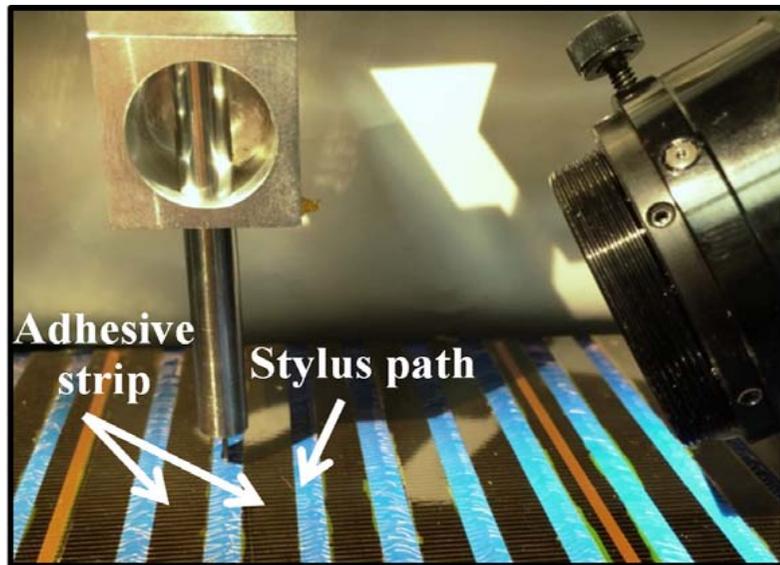


# Direct Cu Plated Bifacial Si-HJT Cells Process Flow



# Measuring Adhesion of Plated Fingers

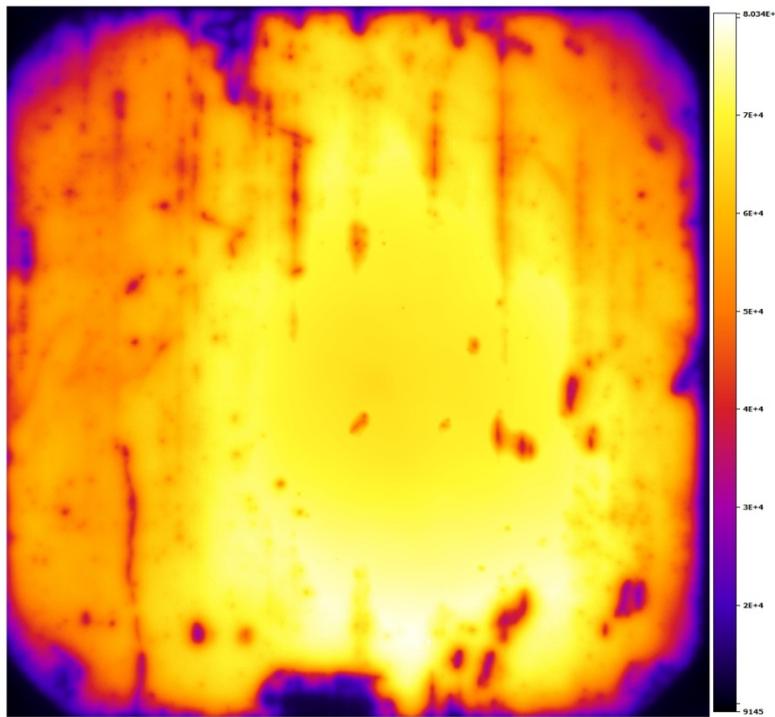
- Use a stylus “scratch tester” to measure the force which is required to either dislodge or cut-off fingers.
- ITO pre-treatment before Cu plating results in cut-off mode being observed.



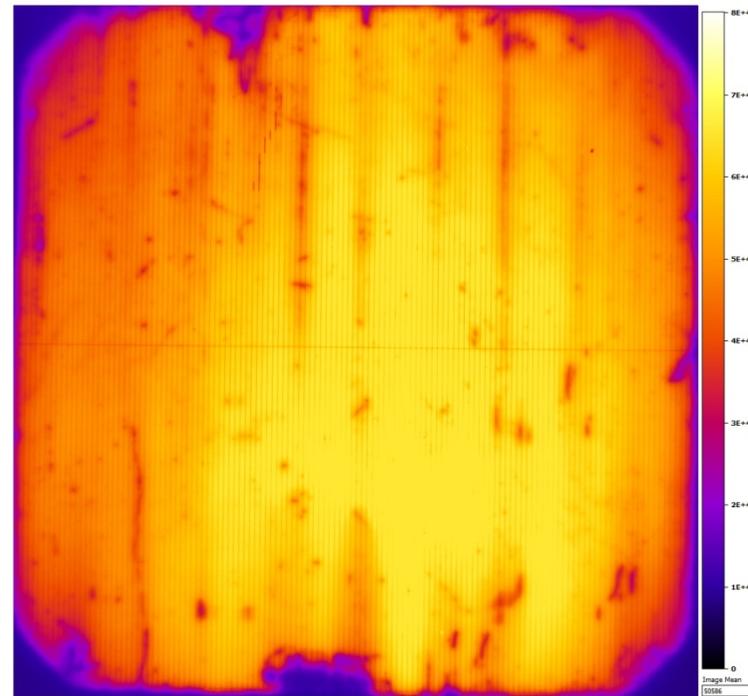
R. Chen et al. (2014) Failure Modes Identified During Adhesion Testing of Metal Fingers on Silicon Solar Cells, Metallisation Workshop 5:20 pm.

# Process Induced Degradation

The patterning and plating processes do not impact cell voltage  
PL images were taken under 5 V and 0.05 s. Maximum value for both images is 80000.



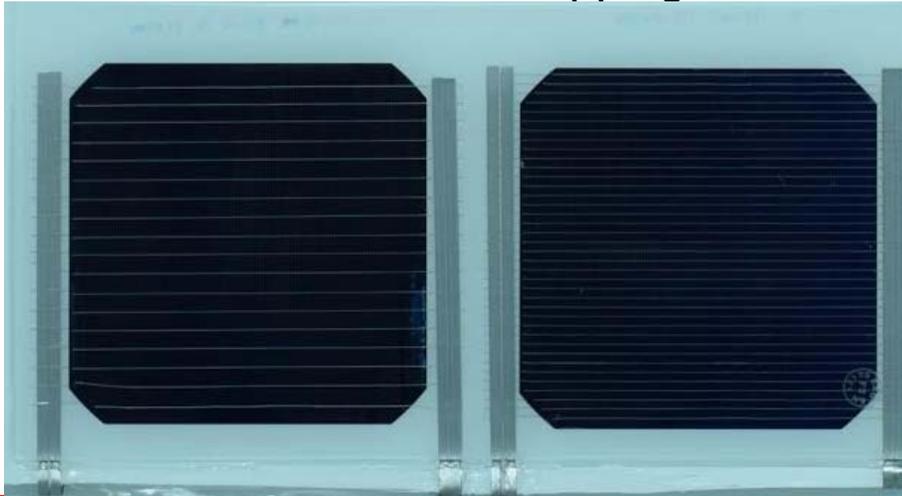
PL for a HJT wafer before processing



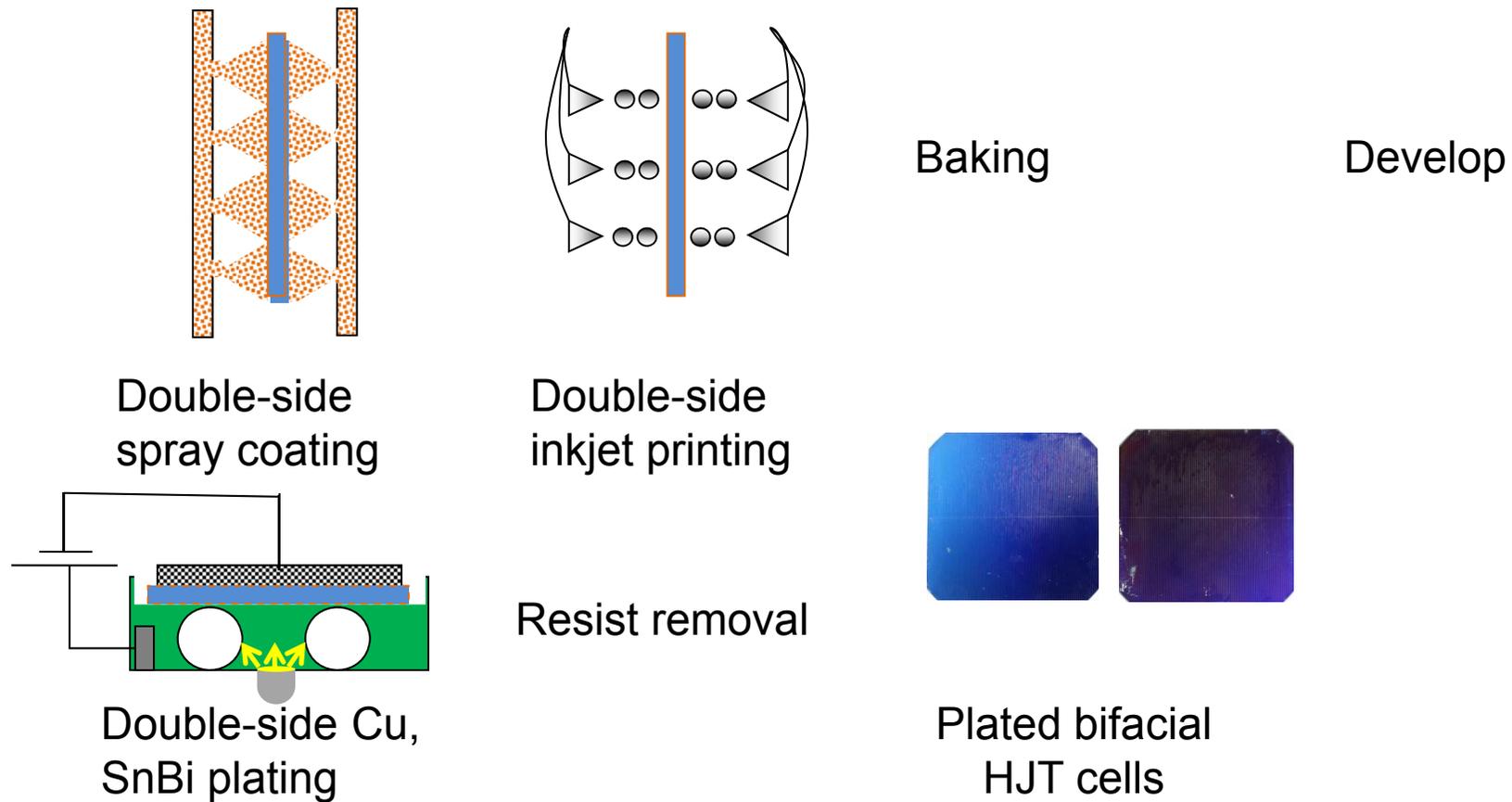
PL for a finished bifacial HJT cell

# Cu Plated Bifacial HJT Module

- Cells were plated with fingers parallel on both sides and no busbars. They were interconnected into SmartWire modules for I-V measurement.
- Maximum mini-module efficiency was 18.8% ( $V_{oc} = 717$  mV,  $J_{sc} = 35.4$  mA/cm<sup>2</sup> and FF = 74 %) .
- FF was only 74% due largely to non uniform Sn capping which allowed Cu oxidation.
- Future work will use SnBi capping with reflow.



# Proposed Process Flow for Bifacial HJT Cells Metallisation



# Conclusions

- A new low cost inkjet patterning technology was reported
  - Patterned line width can be as narrow as 20  $\mu\text{m}$
  - Photo sensitive material and UV exposure can be avoided
  - Only need to print one layer of ink to prevent cross linking.
- Direct Cu plated bifacial Si-HJT mini-modules were demonstrated using the patterning method
  - Good adhesion between the Cu and ITO was achieved
  - Process can be further simplified thereby reducing cost
- Future work will focus on capping the plated Cu fingers with SnBi alloy



Thanks for your attention!